

# **CMOS SRAM Circuit Design And Parametric Test In Nano-Scaled Technologies: Process-Aware SRAM Design And Test (Frontiers In Electronic Testing) By Andrei Pavlov;Manoj Sachdev**

**By Andrei Pavlov;Manoj Sachdev**

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Static random-access memory 3 Design; 4 SRAM operation. 4.1 Bus behavior; 5 See also; 6 References; A six-transistor CMOS SRAM cell.

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