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By Andrei Pavlov;Manoj Sachdev

Static random-access memory 3 Design; 4 SRAM operation. 4.1 Bus behavior; 5 See also; 6 References; A six-transistor CMOS SRAM cell.
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Andrei Pavlov , Manoj Sachdev, CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM nano-CMOS SRAM (static random access
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This book provides a guide to Static Random Access Memory (SRAM) Cmos Sram Circuit Design And Parametric Test design and test issues in nano-scaled
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