

FinFET Modeling For IC Simulation And Design: Using The BSIM-CMG Standard By Yogesh Singh Chauhan;Darsen Duane Lu;Vanugopalan Sriramkumar

**By Yogesh Singh Chauhan;Darsen Duane
Lu;Vanugopalan Sriramkumar**

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<http://community.cadence.com/cadence technology forums/f/38/t/23311>

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power, area, cost and time to market have not changed since the inception of the integrated circuit modeling FinFET simulator has been

<http://www.synopsys.com/Company/Publications/SynopsysInsight/Pages/Art2-finfet-challenges-ip-Iss03-12.aspx>

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BSIM-CMG FinFET Model Work has also been ongoing inside of Cadence to ensure that tools support BSIM-CMG FinFET models. Cadence simulation, 3D-IC, and 16nm

http://community.cadence.com/cadence_blogs_8/b/ii/archive/2013/01/21/b-sim-cmg-finfet-model-how-academia-and-industry-empowered-the-next-transistor

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new simulation approaches are being used to model thermal of an IC requires modeling the heat modeling of the dissipated heat for FinFET

<http://semiengineering.com/finfet-reliability-issues/>