

Power Electronic Packaging: Design, Assembly Process, Reliability And Modeling By Yong Liu

By Yong Liu

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http://en.wikipedia.org/wiki/Electronic_packaging

Challenges of wafer level power semiconductor packaging and modeling design, reliability and assembly process power electronic packaging and modeling

<http://www.sciencedirect.com/science/article/pii/S0026271409003527>

In the integrated circuit industry it is called simply packaging and sometimes semiconductor device assembly, with electronic packaging, electric power than

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IEEE Fellow Dr. Yong Liu, modeling, manufacturing and reliability of power electronic packaging. Blog. He wrote Power Electronic Packaging: Design, Assembly

<http://blog.fairchildsemi.com/2015/ieee-honors-fairchilds-dr-yong-liu-2015-ieee-fellow/>

the entire circuit board assembly to form the electronic to higher power Material Design, 3rd Annual Semiconductor Packaging

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